REMARKS

Reconsideration of the application is respectfully requested.

In the Office Action, claims 5-13 stand rejected as being anticipated by U.S. Patent Application Publication No. 2004/0186688 issued to Nejedlo ("Nejedlo"). Applicants, however, respectfully disagree with the rejection for the following reasons.

Beginning with independent claim 5, this claim recites a memory IC module having a carrier substrate, signal connection points installed on the substrate, and memory devices installed on the substrate. Each memory device has a separate memory core array and separate address decoder logic. A memory buffer is also installed on the substrate and is coupled between the signal connection points and the memory devices. The buffer has a driver circuit whose outputs are coupled to some of the signal connection points. the buffer also has logic to forward read data and determine error in test symbols received from outside the module. Nejedlo does not disclose such a memory IC module.

According to the Office Action at page 3, Nejedlo discloses Applicants' claimed IC module, including a carrier substrate (pointing to Fig. 2 of Nejedlo, units 224, 232). However, Nejedlo associates reference number 224 with **a processor core**. As to unit 232, that is associated with **a memory core**. These elements are not carrier substrates.

In addition, although Nejedlo discloses a computer system equipped with multiple built-in self-tests (BIST) units which are associated with their respective core function circuitry, including memory core 232, Nejedlo does not disclose a memory IC module having a memory buffer that is communicatively coupled between signal connection points on the carrier substrate and a number of memory devices. The Office Action's reference to unit 228 as Applicants' claimed *memory buffer* is improper, because unit 228 cannot be said to be *communicatively coupled between a plurality of first and second signal connection points and a plurality of memory devices*.

According to Nejedlo, unit 228 is a chipset core that is coupled between the memory modules and the processor, and more particularly, between the interconnect bus 243 and 241. Note that according to the Office Action, unit 243 discloses the claimed

plurality of first and second signal connection points installed on the substrate. Assuming that is true, then the Office Action's reference to unit 228 as being *communicatively coupled between the plurality of first and second signal connection points and the plurality of memory devices* is incorrect (assuming that the memory modules of Nejedlo disclose the claimed *plurality of memory devices*).

In addition, the Office Action fails to identify where in Nejedlo unit 228 is taught or suggested as being or having *a memory buffer having a plurality of driver circuits whose outputs are coupled to the plurality of first signal connection points, respectively, and logic to a) forward read data, provided by the memory devices, at speed using the plurality of drivers in a normal mode of operation for the module, and b) determine error in test symbols received from outside the module at speed using the plurality of second signal connection points in a test mode of operation for the module during which a chip-to-chip connection between the module and another device is tested.* Although the chipset 228 may have a buffer that includes driver circuits, this does not teach or suggest modifying the chipset to include Applicants' claimed *memory buffer*.

Turning now to claim 9, this claim recites a system of IC devices comprising *a memory module installed on the carrier substrate to communicate with a host IC device that is also on the substrate, the module having a memory buffer circuit with repeater capability to a) forward address and command information from the memory controller logic to a second main memory module, and b) forward read data from the second main memory module to the memory controller logic wherein the first module has BIST checker logic to determine error in the test symbols transmitted by the BIST generator logic of the host IC device.* Nejedlo does not teach or suggest modifying its memory modules in such a manner.

Although the Office Action refers to units 224, 228 of Nejedlo as allegedly disclosing the claimed *first main memory module installed on the substrate to communicate with the host IC device*, this is an incorrect interpretation of Nejedlo. Nejedlo refers to processor core 224 and chipset core 228, separate from **memory cores 232 that make up the memory modules**. Thus, the Office Action is not considering the teachings of Nejedlo, but instead is improperly using hindsight in attempting to contort the functional elements of Nejedlo so that they can "fit" within Applicants' claim language.

A fair reading of Nejedlo simply does not teach or suggest modifying its memory modules into the form recited in Applicants' claim 9.

Any dependent claims not mentioned above are submitted as being neither anticipated nor obvious in view of Nejedlo, for at least the reasons given above in support of their base claims 5 and 9.

CONCLUSION

In sum, a good faith attempt has been made to explain why the rejection is improper. It is believed that the claims are otherwise in condition for allowance, such that a Notice of Allowance referring to claims 5-13 be issued at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
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Dated: October 6, 2005

By _____
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on October 6, 2005.

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Margaux Rodriguez *October 6, 2005*